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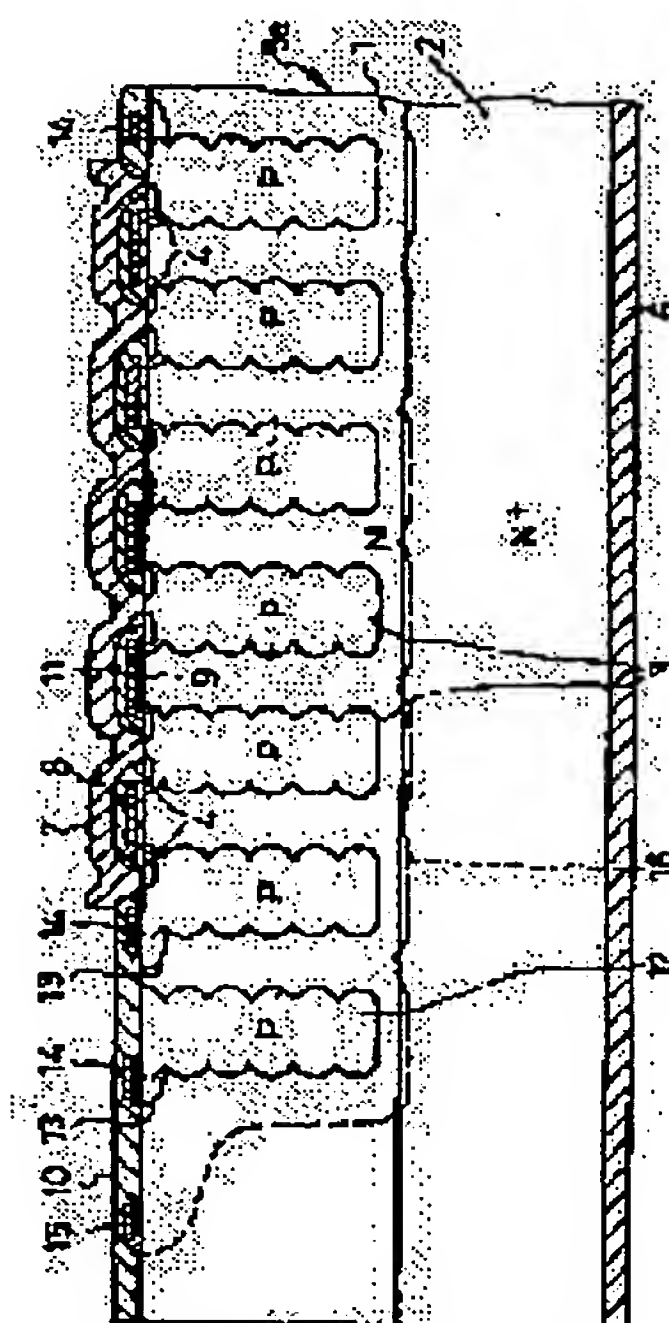
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(54) INSULATED-GATE FIELD-EFFECT TRANSISTOR

(57)Abstract:

PROBLEM TO BE SOLVED: To spread depletion layers to the peripheral sides of FET elements excellently, and to increase the breakdown voltage in the peripheries of the elements, by forming breakdown voltage increasing regions of the same depth as the base regions on the peripheral sides of the base regions, and forming auxiliary regions shallower than the breakdown voltage increasing regions.

SOLUTION: Since each base region 3 is formed into the shape of a pillar in a drift region 1, and the specific resistance of the drift region 1 is set to a relatively small value, the resistance of a current path of the drift region 1 is reduced, and reduction of operating resistance is achieved at a high level. Besides, concerning the breakdown voltage of each element forming region, a sufficiently high breakdown voltage is obtained, since the intervals between base regions 3 are filled with depletion layers 16. Besides, concerning the breakdown voltage on the peripheral side of each element, a sufficiently high breakdown voltage is obtained, since a depletion layer 16 can be spread smoothly so as to lighten field concentration to the peripheral side of the element excellently by a breakdown voltage increasing region 12 and an auxiliary region 13.



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CLAIMS

[Claim(s)]

[Claim 1] The semi-conductor base which has a drain field, a drift region, two or more base regions, two or more source fields, and two or more fields for the improvement in a proof pressure. It has gate dielectric film, a drain electrode, a source electrode, and a gate electrode. Said drift region is arranged so that it may have the part which has high impurity concentration lower than the high impurity concentration of said drain field, and is exposed to one principal plane of said semi-conductor base. Said drain field is arranged between said drift regions and principal planes of another side of said semi-conductor base. Each of two or more of said base regions was distributed by island shape in said drift region, and is prolonged in the shape of a column toward the principal plane of another side from one principal plane of said semi-conductor base. Each of two or more of said emitter regions is arranged in said two or more base regions at island shape. Said two or more fields for the improvement in a proof pressure have the same conductivity type as said base region. The insulated gate field effect transistor characterized by having been formed into said drift region at island shape, and having seen superficially, and having been distributed by the outside of said base region like said base region, and having extended in the shape of a column toward the principal plane of another side from one principal plane of said semi-conductor base.

[Claim 2] Furthermore, it is the insulated gate field effect transistor according to claim 1 characterized by being formed more shallowly [it is arranged and] than said field for the improvement in a proof pressure so that it may have an auxiliary field for assisting the breadth of the depletion layer near said field for the improvement in a proof pressure, and this auxiliary field may have the same conductivity type as said field for the improvement in a proof pressure and it may expose to the front face of said semi-conductor base.

[Claim 3] Said field for the improvement in a proof pressure is an insulated gate field effect transistor according to claim 1 or 2 which has the almost same depth as said base region, and is formed in said base region and coincidence.

[Claim 4] Furthermore, an insulated gate field effect transistor claim 1 characterized by having both a field plate, and equipotential both [either or] so that it may see superficially and said base region may be surrounded, 2, or given in three.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] This invention relates to the insulated gate field effect transistor which can attain high pressure-proofing-ization.

[0002]

[Description of the Prior Art] It is well-known to constitute an insulated gate field effect transistor (for it to be called Following FET), as both reduction-izing of dynamic resistance and high pressure-proofing-ization are shown in drawing 1 for the purpose of attaining excellently. This FET is the N type drift region 1 and N+. It has the silicon semi-conductor base 5 which consists of the mold drain field 2, two or more P type base regions 3, and two or more source fields 4, the drain electrode 6, the source electrode 7, the gate electrode 8, gate dielectric film 9, the circumference protection insulator layer 10, and the interlayer insulation film 11. The base region 3 which can be called the body field of this FET or a channel formation field has a unique configuration, is deeply formed in the thickness direction of a drift region 1 in the shape of a column, and has attained that base to near the interface of a drift region 1 and the drain field 2. If two or more base regions 3 are formed in the shape of a column, when high reverse voltage is impressed to the PN junction between a base region 3 and a drift region 1, the mutual drift region 1 of two or more base regions 3 will be filled by the depletion layer, and pressure-proofing will improve. Moreover, in the case of the structure of drawing 1, even if it makes specific resistance of a drift region 1 small and attains reduction-ization of dynamic resistance, high pressure-proofing can be obtained comparatively. That is, even if it sets the specific resistance of a drift region 1 as conventional conventional $1/3 - 1/5$ of specific resistance of a drift region which have a shallow base region, pressure-proofing equivalent to FET of standard structure can be obtained by work of a depletion layer. [of standard structure] [of FET]

[0003]

[The technical problem which invention makes solution *****] By the way, in this conventional kind of FET, the improvement about the improvement in a proof pressure of the periphery veranda of a component is not fully made. For this reason, the actual condition was not able to attain high pressure-proofing-ization, so that it was expected. That is, even if it diffuses a base region 3 deeply in the thickness direction of a drift region 1 as mentioned above and aims at improvement in a proof pressure of a component central site (component active region), if the pressure-proofing by the side of a component periphery does not improve similarly, the improvement pressure-proofing as the whole component is not attained. Then, the invention-in-this-application person tried to form a well-known field limiting ring (FLR) so that the periphery side of the main junction, i.e., a component active region, may be surrounded, and to aim at improvement in a proof pressure by the side of a component periphery. However, since the specific resistance of a drift region 1 was quite small compared with usual FET in FET of the above-mentioned structure, improvement in a proof pressure was not able to be aimed at with the conventional FLR structure.

[0004] Then, the purpose of this invention is to offer the insulated gate field effect transistor which can attain both reduction, and both [either or] in a proof pressure of dynamic resistance easily and good.

[0005]

[Means for Solving the Problem] This invention for solving the above-mentioned technical problem and attaining the above-mentioned purpose The semi-conductor base which has a drain field, a drift region, two or more base regions, two or more source fields, and two or more fields for the improvement in a proof pressure, It has gate dielectric film, a drain electrode, a source electrode, and a gate electrode. Said drift region is arranged so that it may have the part which has high impurity concentration lower than the high impurity concentration of said drain field, and is exposed to one principal plane of said semi-conductor base. Said drain field is arranged between said drift regions and principal planes of another side of said semi-conductor base. Each of two or more of said base regions was distributed by island shape in said drift region, and is prolonged in the shape of a column toward the principal plane of another side from one principal plane of said semi-conductor base. Each of two or more of said emitter regions is arranged in said two or more base regions at island shape. Said two or more fields for the improvement in a proof pressure have the same conductivity type as said base region. It is a thing concerning the insulated gate field effect transistor characterized by having been formed into said drift region at island shape, and having seen superficially, and having been distributed by the outside of said base region like said base region, and having extended in the shape of a column toward the principal plane of another side from one principal plane of said semi-conductor base. It is.

[0006] In addition, as shown in claim 2, it is desirable to prepare the auxiliary field for helping the breadth of the

depletion layer near the field for the improvement in a proof pressure. This auxiliary field is formed in annular or island shape. Moreover, as shown in claim 3, it is desirable to form the field for the improvement in a proof pressure in the same depth as a base region. Moreover, as shown in claim 4, it is desirable to form a field plate or an equipotential ring (EQR).

[0007]

[Effect of the Invention] According to invention of each claim, circumference pressure-proofing of an FET component can be raised easily and good. That is, although the change width of face of the depletion layer by the side of the periphery of a base region will also become large if a base region is deeply formed in the shape of a column, by preparing the field for the improvement in a proof pressure, change of a depletion layer can be made slow and component circumference pressure-proofing improves good. Moreover, according to invention of claim 2, a depletion layer spreads much more good with the help of an auxiliary field. Moreover, a production process will be simplified, if the field for the improvement in a proof pressure is formed in a base region and coincidence as shown in claim 3. Moreover, if both a field plate, and equipotential both [either or] (EQR) are prepared as shown in claim 4, the breadth of a depletion layer will become still better.

[0008]

[An operation gestalt and an example] Next, with reference to drawing 2 - drawing 7 , the operation gestalt and example of this invention are explained.

[0009]

[The 1st example] The insulated gate field effect transistor (FET) of the 1st example shown in drawing 2 and drawing 3 Have the N type (1st conductivity type) drift region 1, N+ mold drain field 2, the P type (2nd conductivity type) base region 3, the N type source field 4, the drain electrode 6, the source electrode 7, the gate electrode 8, gate dielectric film 9, the circumference protection insulator layer 10, and an interlayer insulation film 11 like conventional FET of drawing 1 , and also The field 12 for the improvement in a P type proof pressure of the shape of a column established into silicon semi-conductor base 5a, and the auxiliary field 13 of P type, It has the field plate 14 prepared into the circumference insulator layer 10, and the equipotential ring 15, i.e., EQR, and is formed in the upper and lower sides and bilateral symmetry focusing on the A-A line and B-B line of drawing 2 .

[0010] A drift region 1 is an N-type semiconductor field, and is N+. It has high impurity concentration lower than the mold drain field 2. In addition, since a drift region 1 has the same conductivity type as the drain field 2, it can also call this a drain field. The drift region 1 consisted of what carried out epitaxial growth of the N-type semiconductor to the multilayer on the drain field 2, and the part has exposed it to one principal plane of semi-conductor base 5a. The high impurity concentration of this drift region 1 is higher than the high impurity concentration of the drift region of conventional FET of the shallow base region which does not form the pillar-shaped base region 3. Therefore, the resistivity of a drift region 1 is conventional conventional $1/5 - 1/3$ of resistivity. [of FET] [of a drift region]

[0011] N+ The mold drain field 2 is arranged between the drift region 1 and the principal plane of another side of semi-conductor base 5a. In addition, the interface of the drain field 2 and a drift region 1 is parallel to the principal plane of another side of plate-like semi-conductor base 5a. The drain electrode 6 consists for example, of a vacuum-plating-of-aluminium layer, and is connected to the drain field 2 in the principal plane of another side of semi-conductor base 5a.

[0012] A base region 3 can also be called a body field or a channel formation field, and is formed in the shape of a column toward the inferior surface of tongue from the top face in the drift region 1. The top face of a base region 3 is exposed to the top face of semi-conductor base 5a, and the inferior surface of tongue of a base region 3 is arranged so that it may estrange a little from the drain field 2. Thus, it is thought by arranging so that it may estrange a little that electric-field concentration with the base region 3 down side can be eased. As shown in drawing 2 , a base region 3 is seen superficially, and is formed in semi-conductor base 5a at island shape, and is distributed by homogeneity, and each base region 3 has a square-like flat-surface configuration. In addition, the flat-surface configuration of a base region 3 is not restricted to a square, but even if it is circular, it is good. This base region 3 repeats and forms a well-known epitaxial growth technique and a well-known diffusion technique. That is, the N-type semiconductor field of closing in is formed with epitaxial growth on the drain field 2, and a P-type semiconductor field is formed in this N-type semiconductor field with a diffusion technique. This P-type semiconductor field constitutes a part of base region, and the N-type semiconductor field of a part in which a P-type semiconductor field is not formed constitutes a part of drift region 1. A P-type semiconductor field is formed by diffusion so that the P-type semiconductor field which formed the P-type semiconductor field, formed the N-type semiconductor field of closing in in the top face of the P-type semiconductor field of cod roe and an N-type semiconductor field with epitaxial growth, and formed it in it previously again may be followed. By repeating this process multiple times (for example, 6 times), column-like a base region 3 and a drift region 1 are formed.

[0013] The N type source field 4 was formed into each base region 3 at island shape, and is exposed to one principal plane of semi-conductor base 5a. Into 16 base regions 3 arranged inside in many base regions 3, a square 4, i.e., an annular source field, is formed, the U-shaped source field 4 is formed into eight base regions 3 on the outside side, and the L character-like source field 4 is formed in eight base regions 3 of an angle. The amount of [between the source fields 4 and drift regions 1 in a base region 3] surface flank becomes a channel formation part.

[0014] The source electrode 7 is the vacuum evaporatio no layer of aluminum, it connects with both each source field 4 and each base region 3, and it is prepared also on the interlayer insulation film 11 so that common connection of two or more source fields 4 may be made.

[0015] Gate dielectric film 9 consists of the silicon oxide formed so that the channel formation part in a base region 3 mentioned above might be covered at least.

[0016] The gate electrode 8 consists of the polycrystalline silicon formed by well-known chemical vapor deposition, and is formed on gate dielectric film 9. This gate electrode 8 is connected to the metal gate terminal which sees superficially, is formed in the shape of a grid, and is not illustrated.

[0017] Many (this example 64 pieces) fields 12 for the improvement in a proof pressure prepared according to this invention are distributed so that it may conclude superficially that it is clear from drawing 2 and a base region 3 may be surrounded. This field 12 for the improvement in a proof pressure is formed in a base region 3 and coincidence, consists of the P type diffusion field which has the same high impurity concentration as a base region 3, and it has the same flat-surface configuration as a base region 3, and the same cross-section configuration, and it is distributed by homogeneity like the base region 3. That is, the field 12 for the improvement in a proof pressure was formed into the drift region 1 at island shape, and has extended in the shape of a column toward the principal plane of another side from one principal plane of semi-conductor base 5a. The tip of this field 12 for the improvement in a proof pressure is N+. It is located near the mold drain field 2. In addition, mutual spacing of two or more fields 12 for the improvement in a proof pressure is the same as mutual spacing of a base region 3.

[0018] The P type auxiliary field 13 which attaches and shows **** in drawing 2 has the same conductivity type as the field 12 for the improvement in a proof pressure, and the same high impurity concentration, and it is annularly formed so that from drawing 2 and the field 12 for the improvement in a proof pressure and a base region 3 may be surrounded. The auxiliary field 13 diffuses a P type impurity in the epitaxial layer of the last of the epitaxial growth of multiple times, and is formed in the maximum upper layer and coincidence of the field 12 for the improvement in a proof pressure, and a base region 3. For this reason, the depth of the auxiliary field 13 is sharply set up shallowly like one sixth (preferably $1/10 - 1/2$) of the depth of the field 12 for the improvement in a proof pressure. In this example, one of the auxiliary fields 13 contacts the periphery side of the field 12 for the improvement in a proof pressure, and one [another] touches the periphery side of the base region 2 by the side of the outermost periphery.

[0019] The field plate 14 is the vacuum evaporatio no layer of aluminum, and it is annularly formed so that the auxiliary field 13 may be countered through an insulator layer 10. That is, the flat-surface configuration of the field plate 14 is almost the same as that of the auxiliary field 13 shown in drawing 2. In the example of drawing 3, the field plate 14 is not electrically connected to the auxiliary field 13, the field 12 for the improvement in a proof pressure, and base region 3 of P type. Moreover, two annular field plates 14 of each other are separated.

[0020] EQR15 is a conductor layer which consists of the vacuum evaporatio no layer of aluminum, and is annularly arranged rather than the auxiliary field 13 at the periphery side. This EQR15 has countered the top face of semi-conductor base 5a through the lower layer of an insulator layer 10, and is not electrically connected to semi-conductor base 5a. In addition, EQR15 also has the function of the channel stopper which it has the function to attain stabilization of the charge of the front face of an insulator layer 10, and also prevents the breadth to the periphery of a depletion layer.

[0021] According to this example, improvement in the proof pressure by the side of the FET component circumference (circumference proof pressure) is achieved, and high pressure-proofing-ization is attained excellently. Moreover, in spite of having formed high pressure-proofing, dynamic resistance (on resistance) can be kept small. That is, since a base region 3 is formed in the shape of a column in a drift region 1 and the specific resistance of a drift region 1 is set up small relatively, resistance of the current path of a drift region 1 can be made small, and reduction-ization of dynamic resistance is attained excellently. Moreover, about pressure-proofing of a component formation field (active region), since it is buried by the depletion layer 16 as between base regions 3 shows drawing 3 typically by the dotted line, sufficiently high pressure-proofing can be obtained. Moreover, about the pressure-proofing by the side of the component circumference, since a depletion layer 16 can be smoothly extended so that electric-field concentration may be eased good to a component periphery side like illustration by the field 12 for the improvement in a proof pressure, and the auxiliary field 13, pressure-proofing high enough can be obtained like a component central site.

[0022] In the condition that the electrical potential difference which forms a channel between the gate electrode 8 and the source electrode 7 is not impressed if it explains in more detail about a spread of a depletion layer 16, if an electrical potential difference with the high sense which carries out the reverse bias of the PN junction between a drift region 1 and a base region 3 is impressed between the drain electrode 6 and the source electrode 7, a depletion layer will spread in the drift region 1 where high impurity concentration is lower than a base region 3. Since many base regions 3 are arranged in the shape of a column, the mutual drift region 1 of a base region 3 is buried with a depletion layer 16. A depletion layer 16 spreads not only in between base regions 3 but in between a base region 3 and the field 12 for the improvement in a proof pressure formed similarly and between this and the base region 3. Although a depletion layer 16 cannot fully be extended only by the field 12 for the improvement in a proof pressure to the periphery side of a base region 3, if the auxiliary field 13 is formed, a depletion layer 16 will spread good by this assistance on the outside of between the fields 12 for the improvement in a proof pressure, between base regions 3, and the field 12 for the improvement in a proof pressure. Moreover, since the auxiliary field 13 is formed more shallowly than the field 12 for the improvement in a proof pressure and is arranged at the periphery side, change of the depletion layer 16 by the side of a periphery becomes slow, and the improvement in a proof pressure is attained good.

[0023] In this example, since the field 12 for the improvement in a proof pressure, and the field plate 14 and EQR15

other than this auxiliary field 13 are prepared, a depletion layer 16 spreads still more stably and good. Moreover, it is prevented by work of EQR15 that a depletion layer 16 spreads to the side face of semi-conductor base 5a, and it can attain high pressure-proofing-ization stably by it. Moreover, since the field 12 for the improvement in a proof pressure is formed in a base region 3 and coincidence in this example, it is advantageous in respect of productivity. [0024]

[The 2nd example] Next, the insulated gate field effect transistor of the 2nd example shown in drawing 4 is explained. However, in drawing 4 and drawing 5 mentioned later - drawing 7, the same sign is substantially given to the same part with drawing 2 and drawing 3, and the explanation is omitted.

[0025] FET of drawing 4 is constituted identically to the 1st example except for arrangement of P type auxiliary field 13a. Auxiliary field 13a of drawing 4 is estranged to the periphery side corresponding to the auxiliary field 13 of drawing 3 from the field 12 for the improvement in a proof pressure, and the base region 3. In addition, the flat-surface configuration of auxiliary field 13a of drawing 4 is annular like drawing 2, and the depth is the same as that of the auxiliary field 13 of drawing 3. The same effectiveness as the 1st example can be acquired also according to this 2nd example.

[0026]

[The 3rd example] Drawing 5 shows a part of front face of semi-conductor base 5a of FET of the 3rd example. FET of the 3rd example of drawing 5 is constituted identically to the 1st example except for P type auxiliary field 13b which attaches **** and is shown explanatorily. P type auxiliary field 13b of drawing 5 prepared for the same purpose as the auxiliary field 13 of the 1st example consists of many island-shape fields. Auxiliary field 13b has the same depth as the auxiliary field 13 of the 1st example, and the same high impurity concentration, and is distributed between the field 12 for the improvement in a proof pressure, and the base region 3 by the side of the outermost periphery. Drawing 6 R> 6 shows the physical relationship of the field 12 for the improvement in a proof pressure, and auxiliary field 13b. Auxiliary field 13b is arranged so that the core of auxiliary field 13b may be in agreement with the core of the square of a dotted line of from now on connecting the core of four fields 12 for the improvement in a proof pressure so that clearly. Moreover, auxiliary field 13b is arranged so that the minimum distance L of square auxiliary field 13b and four fields 12 for the improvement in a proof pressure may become almost respectively the same. In addition, the relation between a base region 3 and auxiliary field 13b is the same as that of drawing 6.

[0027] By arranging auxiliary field 13b, as shown in drawing 6, a depletion layer can be extended good between the fields 12 for the improvement in a proof pressure, and between the base region 3 by the side of the outermost periphery, and the field 12 for the improvement in a proof pressure, and the improvement in a proof pressure is attained like the 1st example.

[0028]

[Modification(s)] This invention is not limited to an above-mentioned example, and the next deformation is possible for it.

- (1) The field plate 14 is electrically connectable with the auxiliary field 13 or the field 12 for the improvement in a proof pressure, as shown in drawing 7. Thus, connection raises the equipotential nature of the auxiliary field 13 or the field 12 for the improvement in a proof pressure.
- (2) As shown in drawing 7 R> 7, a level difference can be prepared in the insulator layer 10 of field plate 14 part, and a periphery side can be thickened. More nearly thereby, in a periphery side, the effectiveness of a field plate falls and the change by the side of the periphery of a depletion layer becomes smooth. Moreover, the field plate 14 can be made to extend in a periphery side rather than the auxiliary field 13 or the field 12 for the improvement in a proof pressure, as shown in drawing 7.
- (3) As shown in drawing 7, it is N+ to the periphery edge of semi-conductor base 5a. Mold semiconductor region 1a can be formed and EQR15 can be connected here electrically. Thereby, it is the breadth of a depletion layer N+ It can protect certainly by mold semiconductor region 1a.
- (4) N+ A P type field can be arranged in the mold drain field 2, and it can be made universal contact structure.
- (5) Although the example showed the example by which the base region 3 and the field 12 for the improvement in a proof pressure located the core in the top-most vertices of the virtual square to which these cores are connected, and have been arranged, a base region 3 and the field 12 for the improvement in a proof pressure locate the core in the top-most vertices of the virtual triangle and rhombus which connect these cores, and may arrange.
- (6) The high impurity concentration of the surface exposure parts of a base region 3, the field 12 for the improvement in a proof pressure, and the auxiliary field 13 may be set up highly alternatively.
- (7) The die length which begins to be prolonged outside can be set as arbitration according to the level of the pressure-proofing demanded from the improvement field 12 in a proof pressure of the auxiliary field 13.
- (8) In the example, although the field 12 for the improvement in a proof pressure was considered as the same arrangement as a base region 3, in order to heighten an electric-field relaxation effect, the field 12 for the improvement in a proof pressure can also be precisely arranged compared with a base region 2. Moreover, only the field 12 for the improvement in a proof pressure of the most inner circumference which comes out of all arrangement of the field 12 for the improvement in a proof pressure, and does not make it the same, for example, surrounds a base region 2 can also be precisely arranged compared with other fields 12 for the improvement in a proof pressure.
- (9) It can also consider as the structure where the auxiliary field 13 is not established in the outside of the field 12 for the improvement in a proof pressure of the outermost periphery. Moreover, two or more auxiliary fields 13 can also be established in the outside of the field 12 for the improvement in a proof pressure.

(10) A base region 3 and the field 12 for the improvement in a proof pressure can also be made into the substantial straight configuration which does not have a wen on the side face.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is the sectional view showing conventional FET.

[Drawing 2] It is the top view showing the front face of the semi-conductor base of FET of the 1st example.

[Drawing 3] It is the sectional view showing a part of FET of the 1st example by the A-A line of drawing 2 .

[Drawing 4] It is the sectional view showing a part of FET of the 2nd example with drawing 3 similarly.

[Drawing 5] It is the top view showing a part of front face of the semi-conductor base of FET of the 3rd example.

[Drawing 6] It is the top view expanding and showing a part of drawing 5 .

[Drawing 7] It is the sectional view showing a part of FET of a modification.

[Description of Notations]

- 1 Drift Region
- 2 Drain Field
- 3 Base Region
- 4 Source Field
- 5a Semi-conductor base
- 12 Field for Improvement in Proof Pressure
- 13 Auxiliary Field
- 14 Field Plate
- 15 EQR

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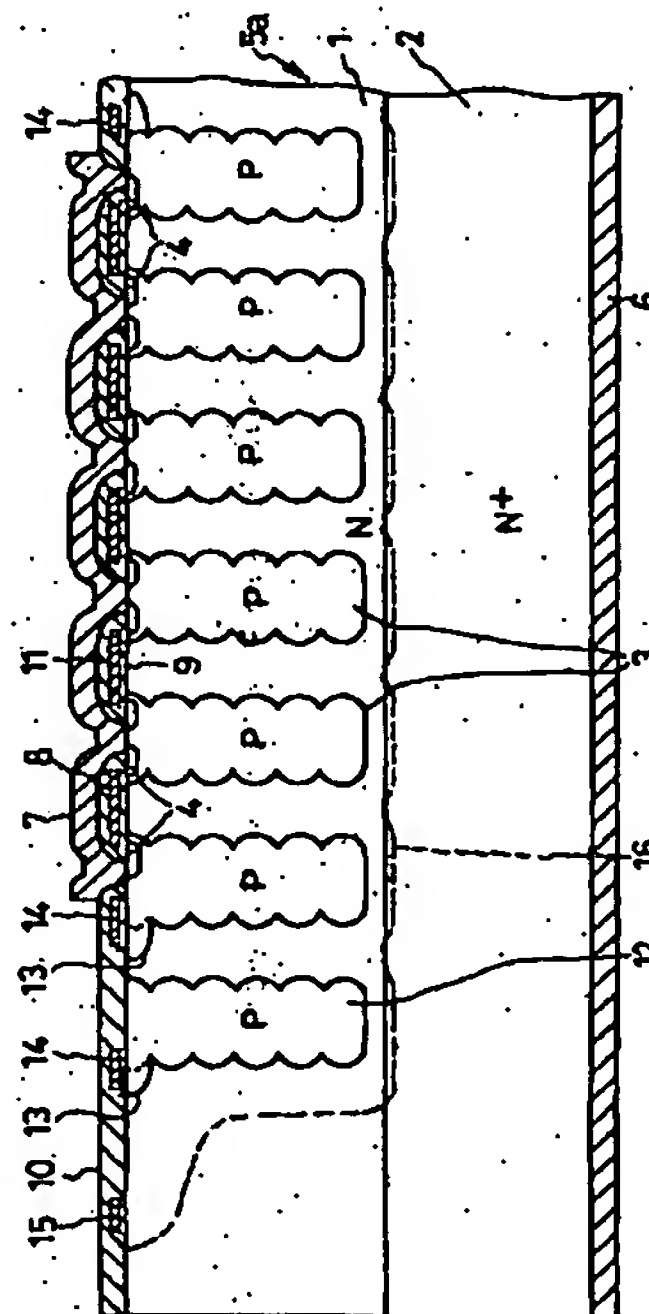
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(54)【発明の名称】 絶縁ゲート型電界効果トランジスタ

(57)【要約】

【課題】 絶縁ゲート型電界効果トランジスタの高耐圧化が困難であった。

【解決手段】 多数のP型柱状ベース領域3をN型ドリフト領域1に設けると共に、柱状ベース領域3の外側に柱状のP型耐圧向上用領域12を設ける。耐圧向上用領域12よりも浅いP型の補助領域13を設ける。空乏層16をベース領域3の外周側に良好に形成して耐圧を高める。



【特許請求の範囲】

【請求項1】 ドレイン領域とドリフト領域と複数のベース領域と複数のソース領域と複数の耐圧向上用領域とを有する半導体基体と、ゲート絶縁膜と、ドレイン電極と、ソース電極と、ゲート電極とを備え、前記ドリフト領域は前記ドレイン領域の不純物濃度よりも低い不純物濃度を有し且つ前記半導体基体の一方の主面に露出する部分を有するように配置され、前記ドレイン領域は前記ドリフト領域と前記半導体基体の他方の主面との間に配置され、前記複数のベース領域のそれぞれは前記ドリフト領域の中に島状に分散配置され且つ前記半導体基体の一方の主面から他方の主面に向かって柱状に延びており、前記複数のエミッタ領域のそれぞれは前記複数のベース領域の中に島状に配置され、前記複数の耐圧向上用領域は前記ベース領域と同一の導電型を有して前記ドリフト領域の中に島状に形成され且つ平面的に見て前記ベース領域の外側に前記ベース領域と同様に分散配置され且つ前記半導体基体の一方の主面から他方の主面に向かって柱状に延びていることを特徴とする絶縁ゲート型電界効果トランジスタ。

【請求項2】 更に、前記耐圧向上用領域の近傍の空乏層の広がり補助するための補助領域を有し、この補助領域は前記耐圧向上用領域と同一の導電型を有し且つ前記半導体基体の表面に露出するように配置され且つ前記耐圧向上用領域よりも浅く形成されていることを特徴とする請求項1記載の絶縁ゲート型電界効果トランジスタ。

【請求項3】 前記耐圧向上用領域は前記ベース領域とほぼ同じ深さを有し、前記ベース領域と同時に形成されたものである請求項1又は2記載の絶縁ゲート型電界効果トランジスタ。

【請求項4】 更に、平面的に見て前記ベース領域を囲むようにフィールドプレートと等電位リングとのいずれか一方又は両方を有することを特徴とする請求項1又は2又は3記載の絶縁ゲート型電界効果トランジスタ。

【発明の詳細な説明】

【0001】

【発明の属する技術分野】本発明は、高耐圧化を達成することができる絶縁ゲート型電界効果トランジスタに関する。

【0002】

【従来の技術】動作抵抗の低減化と高耐圧化の両方を高水準に達成することを目的として絶縁ゲート型電界効果トランジスタ（以下FETと言う）を図1に示すように構成することは公知である。このFETは、N型ドリフト領域1とN⁺型ドレイン領域2と複数のP型ベース領域3と複数のソース領域4とから成るシリコン半導体基体5と、ドレイン電極6と、ソース電極7と、ゲート電極8と、ゲート絶縁膜9と、周辺保護絶縁膜10と、層

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間絶縁膜11とを備えている。このFETのボディ領域又はチャネル形成領域と呼ぶことのできるベース領域3は特異な形状を有し、ドリフト領域1の厚み方向に深く柱状に形成されており、その底面はドリフト領域1とドレイン領域2との界面近くまで達している。複数のベース領域3を柱状に形成すると、ベース領域3とドリフト領域1との間のPN接合に高い逆方向電圧が印加された時に複数のベース領域3の相互間のドリフト領域1が空乏層によって埋められ、耐圧が向上する。また、図1の構造の場合、ドリフト領域1の比抵抗を小さくして動作抵抗の低減化を図っても比較的高耐圧を得ることができ、即ち、ドリフト領域1の比抵抗を、浅いベース領域を有する従来の標準的な構造のFETのドリフト領域の比抵抗の1/3～1/5に設定しても、空乏層の働きで標準的な構造のFETと同等の耐圧を得ることができ

【0003】

【発明が解決しようとする課題】ところで、従来のこの種のFETでは、素子の外周縁側の耐圧向上に関しての改善が十分になされていない。このため、期待されるほど高耐圧化が図れないのが実情であった。即ち、上記のようにベース領域3をドリフト領域1の厚み方向に深く拡散して素子中央側（素子活性領域）の耐圧向上を図っても、素子周縁側の耐圧も同様に向上しなければ素子全体としての向上耐圧は達成されない。そこで、本願発明者は、主接合即ち素子活性領域の外周側を包囲するように周知のフィールドロミッティングリング（FLR）を形成して、素子周縁側の耐圧向上を図ることを試みた。しかしながら、上記構造のFETではドリフト領域1の比抵抗が通常のFETに比べてかなり小さくなっているため、従来のFLR構造では、耐圧向上を図ることができなかった。

【0004】そこで、本発明の目的は、動作抵抗の低減と耐圧向上とのいずれか一方又は両方を容易且つ良好に達成することができる絶縁ゲート型電界効果トランジスタを提供することにある。

【0005】

【課題を解決するための手段】上記課題を解決し、上記目的を達成するための本発明は、ドレイン領域とドリフト領域と複数のベース領域と複数のソース領域と複数の耐圧向上用領域とを有する半導体基体と、ゲート絶縁膜と、ドレイン電極と、ソース電極と、ゲート電極とを備え、前記ドリフト領域は前記ドレイン領域の不純物濃度よりも低い不純物濃度を有し且つ前記半導体基体の一方の主面に露出する部分を有するように配置され、前記ドレイン領域は前記ドリフト領域と前記半導体基体の他方の主面との間に配置され、前記複数のベース領域のそれぞれは前記ドリフト領域の中に島状に分散配置され且つ前記半導体基体の一方の主面から他方の主面に向かって柱状に延びており、前記複数のエミッタ領域のそれぞれは

前記複数のベース領域の中に島状に配置され、前記複数の耐圧向上用領域は前記ベース領域と同一の導電型を有して前記ドリフト領域の中に島状に形成され且つ平面的に見て前記ベース領域の外側に前記ベース領域と同様に分散配置され且つ前記半導体基体の一方の主面から他方の主面に向かって柱状に延びていることを特徴とする絶縁ゲート型電界効果トランジスタに係わるものである。

【0006】なお、請求項2に示すように、耐圧向上用領域の近傍の空乏層の広がりをおけるための補助領域を設けることが望ましい。この補助領域は、例えば環状又は島状に形成する。また、請求項3に示すように、耐圧向上用領域をベース領域と同じ深さに形成することが望ましい。また、請求項4に示すように、フィールドプレート又は等電位リング(EQR)を形成することが望ましい。

【0007】

【発明の効果】各請求項の発明によればFET素子の周辺耐圧を容易且つ良好に向上させることができる。即ち、ベース領域を柱状に深く形成すると、ベース領域の外周側における空乏層の変化幅も大きくなるが、耐圧向上用領域を設けることによって空乏層の変化を緩慢にすることができ、素子周辺耐圧が良好に向上する。また、請求項2の発明によれば、補助領域の助けで空乏層が一層良好に広がる。また、請求項3に示すように耐圧向上用領域をベース領域と同時に形成すると、製造工程が簡略化される。また、請求項4に示すようにフィールドプレートと等電位リング(EQR)とのいずれか一方又は両方を設けると、空乏層の広がりが更に良好になる。

【0008】

【実施形態及び実施例】次に、図2～図7を参照して本発明の実施形態及び実施例を説明する。

【0009】

【第1の実施例】図2及び図3に示す第1の実施例の絶縁ゲート型電界効果トランジスタ(FET)は、図1の従来のFETと同様にN型(第1導電型)ドリフト領域1とN⁺型ドレイン領域2とP型(第2導電型)ベース領域3とN型ソース領域4とドレイン電極6とソース電極7とゲート電極8とゲート絶縁膜9と周辺保護絶縁膜10と層間絶縁膜11とを有する他に、シリコン半導体基体5aの中に設けられた柱状のP型耐圧向上用領域12及びP型の補助領域13と、周辺絶縁膜10の中に設けたフィールドプレート14及び等電位リング即ちEQR15とを有し、図2のA-A線及びB-B線を中心に上下及び左右対称に形成されている。

【0010】ドリフト領域1はN型半導体領域であってN⁺型ドレイン領域2よりも低い不純物濃度を有する。なお、ドリフト領域1はドレイン領域2と同一導電型を有するので、これをドレイン領域と呼ぶこともできる。ドリフト領域1はドレイン領域2の上にN型半導体を多層にエピタキシャル成長させたものから成り、その一部

は半導体基体5aの一方の主面に露出している。このドリフト領域1の不純物濃度は、柱状ベース領域3を形成しない浅いベース領域の従来のFETのドリフト領域の不純物濃度よりは高い。従って、ドリフト領域1の抵抗率は従来のFETのドリフト領域の抵抗率の1/5～1/3である。

【0011】N⁺型ドレイン領域2はドリフト領域1と半導体基体5aの他方の主面との間に配置されている。なお、ドレイン領域2とドリフト領域1との境界面は平板状半導体基体5aの他方の主面に平行である。ドレイン電極6は例えばアルミニウム蒸着層から成り、半導体基体5aの他方の主面においてドレイン領域2に接続されている。

【0012】ベース領域3は、ボディ領域又はチャネル形成領域とも呼ぶことができるものであって、ドリフト領域1内にその上面から下面に向かって柱状に形成されている。ベース領域3の上面は半導体基体5aの上面に露出しており、ベース領域3の下面はドレイン領域2から若干離間するように配置されている。このように若干離間するように配置することによってベース領域3の下側での電界集中を緩和できると考えられる。図2に示すように、ベース領域3は平面的に見て半導体基体5a内に島状に形成され且つ均一に分散配置されており、各々のベース領域3は四角形状の平面形状を有する。なお、ベース領域3の平面形状は四角形に限られず、円形にしてもよい。このベース領域3は、周知のエピタキシャル成長技術と拡散技術とを繰り返して形成する。即ち、ドレイン領域2の上に肉薄のN型半導体領域をエピタキシャル成長によって形成し、このN型半導体領域に拡散技術によってP型半導体領域を形成する。このP型半導体領域はベース領域の一部を構成し、P型半導体領域の形成されていない部分のN型半導体領域はドリフト領域1の一部を構成する。P型半導体領域を形成したらこのP型半導体領域とN型半導体領域の上面に再び肉薄のN型半導体領域をエピタキシャル成長によって形成し、先に形成したP型半導体領域と連続するようにP型半導体領域を拡散によって形成する。この工程を複数回(例えば6回)繰り返すことで、柱状のベース領域3とドリフト領域1が形成される。

【0013】N型ソース領域4は各ベース領域3の中に島状に形成され、半導体基体5aの一方の主面に露出している。多数のベース領域3の中で内側に配置された16個のベース領域3の中には四角形即ち環状のソース領域4が形成され、外側の边上の8個のベース領域3の中にはコ字状のソース領域4が形成され、角の8個のベース領域3の中にはL字状のソース領域4が形成されている。ベース領域3におけるソース領域4とドリフト領域1との間の表面側部分がチャネル形成部分となる。

【0014】ソース電極7は、例えばアルミニウムの蒸着層であって、各ソース領域4と各ベース領域3との両

方に接続され、複数のソース領域4を共通接続するように層間絶縁膜11の上にも設けられている。

【0015】ゲート絶縁膜9は少なくともベース領域3における前述したチャネル形成部分を覆うように形成されたシリコン酸化膜から成る。

【0016】ゲート電極8は、例えば周知の化学的気相成長法で形成された多結晶シリコンから成り、ゲート絶縁膜9の上に形成されている。このゲート電極8は平面的に見て格子状に形成され、図示されていない金属製ゲート端子に接続されている。

【0017】本発明に従って設けられた多数（この実施例では64個）の耐圧向上用領域12は、図2から明らかなように平面的に見てベース領域3を囲むように分散配置されている。この耐圧向上用領域12はベース領域3と同時に形成されたものであって、ベース領域3と同一の不純物濃度を有するP型拡散領域から成り且つベース領域3と同一平面形状及び同一断面形状を有し、且つベース領域3と同様に均一に分散配置されている。即ち、耐圧向上用領域12はドリフト領域1の中に島状に形成され、半導体基体5aの一方の主面から他方の主面

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7225 7230 7235 7240 7245 7250 7255 7260 7265 7270 7275 7280 7285 7290 7295 7300 7305 7310 7315 7320 7325 7330 7335 7340 7345 7350 7355 7360 7365 7370 7375 7380 7385 7390 7395 7400 7405 7410 7415 7420 7425 7430 7435 7440 7445 7450 7455 7460 7465 7470 7475 7480 7485 7490 7495 7500 7505 7510 7515 7520 7525 7530 7535 7540 7545 7550 7555 7560 7565 7570 7575 7580 7585 7590 7595 7600 7605 7610 7615 7620 7625 7630 7635 7640 7645 7650 7655 7660 7665 7670 7675 7680 7685 7690 7695 7700 7705 7710 7715 7720 7725 7730 7735 7740 7745 7750 7755 7760 7765 7770 7775 7780 7785 7790 7795 7800 7805 7810 7815 7820 7825 7830 7835 7840 7845 7850 7855 7860 7865 7870 7875 7880 7885 7890 7895 7900 7905 7910 7915 7920 7925 7930 7935 7940 7945 7950 7955 7960 7965 7970 7975 7980 7985 7990 7995 8000 8005 8010 8015 8020 8025 8030 8035 8040 8045 8050 8055 8060 8065 8070 8075 8080 8085 8090 8095 8100 8105 8110 8115 8120 8125 8130 8135 8140 8145 8150 8155 8160 8165 8170 8175 8180 8185 8190 8195 8200 8205 8210 8215 8220 8225 8230 8235 8240 8245 8250 8255 8260 8265 8270 8275 8280 8285 8290 8295 8300 8305 8310 8315 8320 8325 8330 8335 8340 8345 8350 8355 8360 8365 8370 8375 8380 8385 8390 8395 8400 8405 8410 8415 8420 8425 8430 8435 8440 8445 8450 8455 8460 8465 8470 8475 8480 8485 8490 8495 8500 8505 8510 8515 8520 8525 8530 8535 8540 8545 8550 8555 8560 8565 8570 8575 8580 8585 8590 8595 8600 8605 8610 8615 8620 8625 8630 8635 8640 8645 8650 8655 8660 8665 8670 8675 8680 8685 8690 8695 8700 8705 8710 8715 8720 8725 8730 8735 8740 8745 8750 8755 8760 8765 8770 8775 8780 8785 8790 8795 8800 8805 8810 8815 8820 8825 8830 8835 8840 8845 8850 8855 8860 8865 8870 8875 8880 8885 8890 8895 8900 8905 8910 8915 8920 8925 8930 8935 8940 8945 8950 8955 8960 8965 8970 8975 8980 8985 8990 8995 9000 9005 9010 9015 9020 9025 9030 9035 9040 9045 9050 9055 9060 9065 9070 9075 9080 9085 9090 9095 9100 9105 9110 9115 9120 9125 9130 9135 9140 9145 9150 9155 9160 9165 9170 9175 9180 9185 9190 9195 9200 9205 9210 9215 9220 9225 9230 9235 9240 9245 9250 9255 9260 9265 9270 9275 9280 9285 9290 9295 9300 9305 9310 9315 9320 9325 9330 9335 9340 9345 9350 9355 9360 9365 9370 9375 9380 9385 9390 9395 9400 9405 9410 9415 9420 9425 9430 9435 9440 9445 9450 9455 9460 9465 9470 9475 9480 9485 9490 9495 9500 9505 9510 9515 9520 9525 9530 9535 9540 9545 9550 9555 9560 9565 9570 9575 9580 9585 9590 9595 9600 9605 9610 9615 9620 9625 9630 9635 9640 9645 9650 9655 9660 9665 9670 9675 9680 9685 9690 9695 9700 9705 9710 9715 9720 9725 9730 9735 9740 9745 9750 9755 9760 9765 9770 9775 9780 9785 9790 9795 9800 9805 9810 9815 9820 9825 9830 9835 9840 9845 9850 9855 9860 9865 9870 9875 9880 9885 9890 9895 9900 9905 9910 9915 9920 9925 9930 9935 9940 9945 9950 9955 9960 9965 9970 9975 9980 9985 9990 9995 10000 10005 10010 10015 10020 10025 10030 10035 10040 10045 10050 10055 10060 10065 10070 10075 10080 10085 10090 10095 10100 10105 10110 10115 10120 10125 10130 10135 10140 10145 10150 10155 10160 10165 10170 10175 10180 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ゲート型電界効果トランジスタを説明する。但し、図4及び後述する図5～図7において図2及び図3と実質的に同一の部分には同一の符号を付してその説明を省略する。

【0025】図4のFETはP型補助領域13aの配置を除いて第1の実施例と同一に構成されている。図4の補助領域13aは図3の補助領域13に対応するものであって、耐圧向上用領域12及びベース領域3から外周側に離間している。なお、図4の補助領域13aの平面形状は図2と同様に環状であり、また深さは図3の補助領域13と同一である。この第2の実施例によっても第1の実施例と同一の効果を得ることができる。

【0026】

【第3の実施例】図5は第3の実施例のFETの半導体基体5aの表面の一部を示す。図5の第3の実施例のFETは、点々を付して説明的に示すP型補助領域13bを除いて第1の実施例と同一に構成されている。第1の実施例の補助領域13と同一の目的で設けられた図5のP型補助領域13bは多数の島状領域から成る。補助領域13bは第1の実施例の補助領域13と同一の深さ、同一の不純物濃度を有し、耐圧向上用領域12及び最外周側のベース領域3の相互間に分散配置されている。図6は耐圧向上用領域12と補助領域13bとの位置関係を示すものである。これから明らかなように4個の耐圧向上用領域12の中心を結ぶ点線の四角形の中心に補助領域13bの中心が一致するように補助領域13bが配置されている。また、四角形の補助領域13bと4つの耐圧向上用領域12との最短距離Lがそれぞれほぼ同一になるように補助領域13bが配置されている。なお、ベース領域3と補助領域13bとの関係も図6と同様である。

【0027】図6に示すように補助領域13bを配置することによって、耐圧向上用領域12の相互間及び最外周側のベース領域3と耐圧向上用領域12との間に空乏層を良好に広げることができ、耐圧向上が第1の実施例と同様に達成される。

【0028】

【変形例】本発明は上述の実施例に限定されるものではなく、例えば次の変形が可能なものである。

(1) フィールドプレート14を図7に示すように補助領域13又は耐圧向上用領域12に電気的に接続することができる。この様に接続すると、補助領域13又は耐圧向上用領域12の等電位性が向上する。

(2) フィールドプレート14部分の絶縁膜10を図7に示すように段差を設け、外周側を厚くすることができる。これにより、外周側ほどフィールドプレートの効果が低下し、空乏層の外周側での変化が滑らかになる。また、図7に示すようにフィールドプレート14を補助領域13又は耐圧向上用領域12よりも外周側に延在させることができる。

(3) 図7に示すように半導体基体5aの外周縁にN⁺型半導体領域1aを形成し、ここにEQR15を電気的に接続することができる。これにより、空乏層の広がりやN⁺型半導体領域1aで確実に防ぐことができる。

(4) N⁺型ドレイン領域2の中にP型領域を配置してユニバーサルコンタクト構造にすることができる。

(5) 実施例では、ベース領域3及び耐圧向上用領域12がこれらの中心を結ぶ仮想四角形の頂点にその中心を位置させて配置された例を示したが、ベース領域3及び耐圧向上用領域12がこれらの中心を結ぶ仮想三角形やひし形の頂点にその中心を位置させて配置してもよい。

(6) ベース領域3、耐圧向上用領域12及び補助領域13の表面露出部分の不純物濃度を選択的に高く設定してもよい。

(7) 補助領域13の耐圧向上用領域12から外側に延び出す長さは、要求される耐圧のレベルに応じて任意に設定することができる。

(8) 実施例では、耐圧向上用領域12をベース領域3と同一の配置としたが、電界緩和効果を高める為に耐圧向上用領域12をベース領域2に比べて緻密に配置することもできる。また、耐圧向上用領域12の配置を全てで同じにせず、例えばベース領域2を包囲する最内周の耐圧向上用領域12のみ他の耐圧向上用領域12に比べて緻密に配置することもできる。

(9) 最外周の耐圧向上用領域12の外側には、補助領域13を設けない構造とすることもできる。又、耐圧向上用領域12の外側に複数本の補助領域13を設けることもできる。

(10) ベース領域3及び耐圧向上用領域12を、その側面にこぶを有しない実質的なストレートな形状とすることもできる。

【図面の簡単な説明】

【図1】従来のFETを示す断面図である。

【図2】第1の実施例のFETの半導体基体の表面を示す平面図である。

【図3】第1の実施例のFETの一部を図2のA-A線で示す断面図である。

【図4】第2の実施例のFETの一部を図3と同様に示す断面図である。

【図5】第3の実施例のFETの半導体基体の表面の一部を示す平面図である。

【図6】図5の一部を拡大して示す平面図である。

【図7】変形例のFETの一部を示す断面図である。

【符号の説明】

1 ドリフト領域

2 ドレイン領域

3 ベース領域

4 ソース領域

50 5a 半導体基体

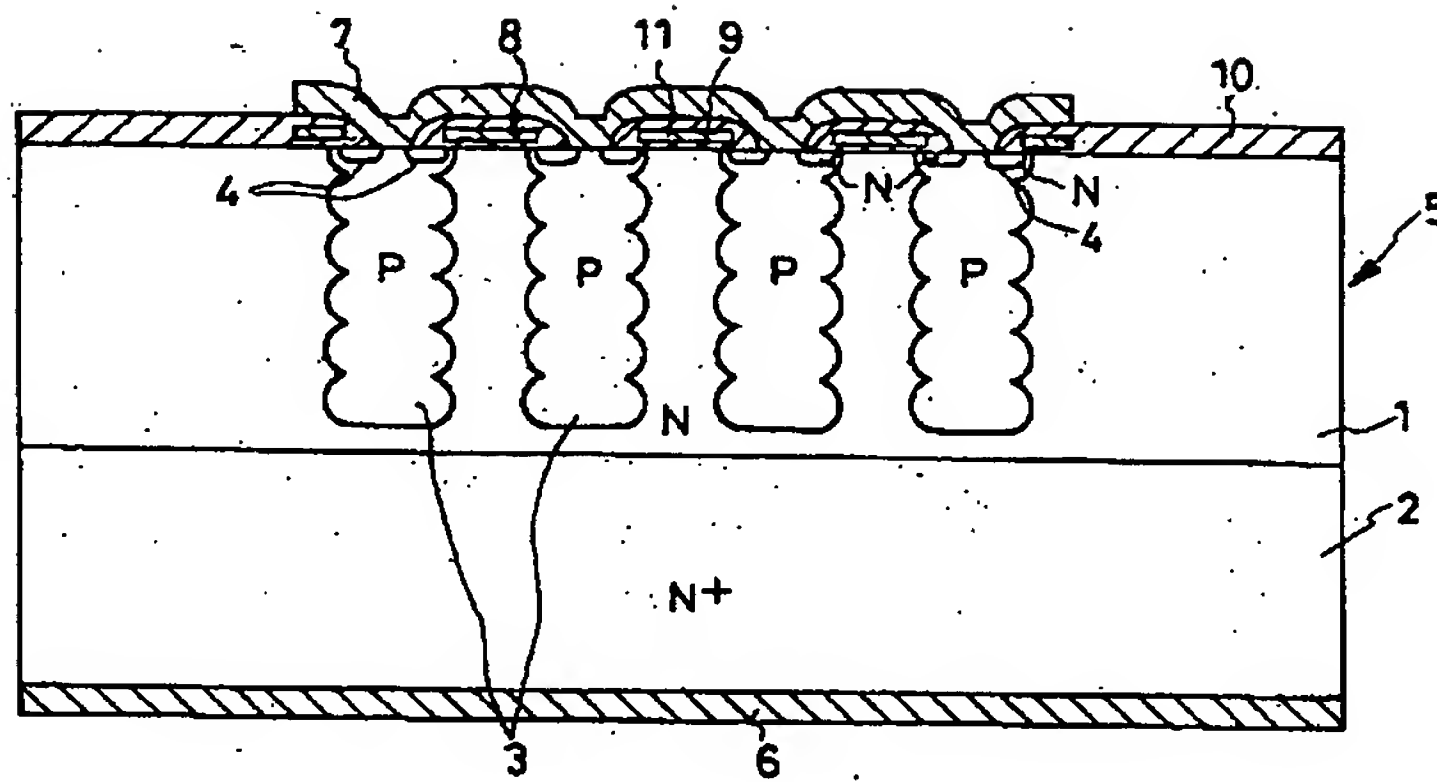
1 2 耐圧向上用領域

1 3 補助領域

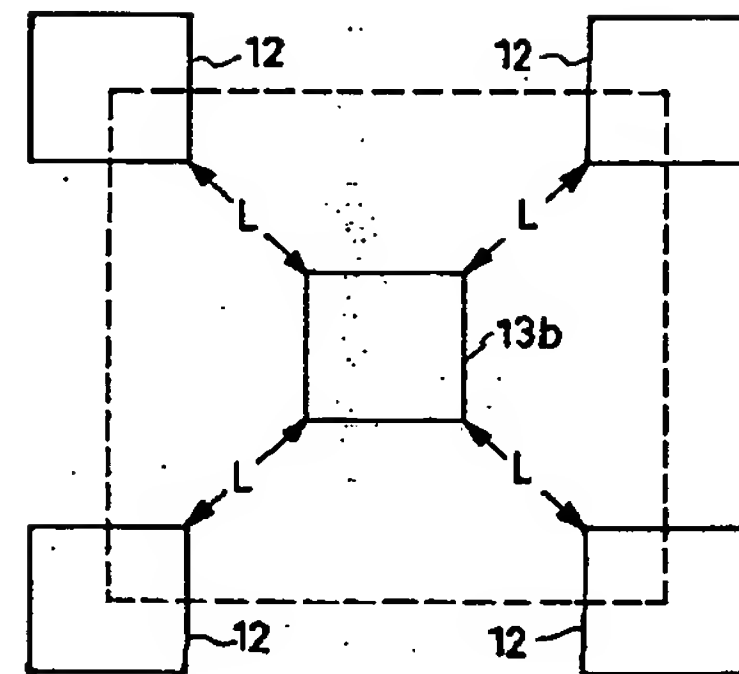
* 1 4 フィールドプレート

* 1 5 EQR

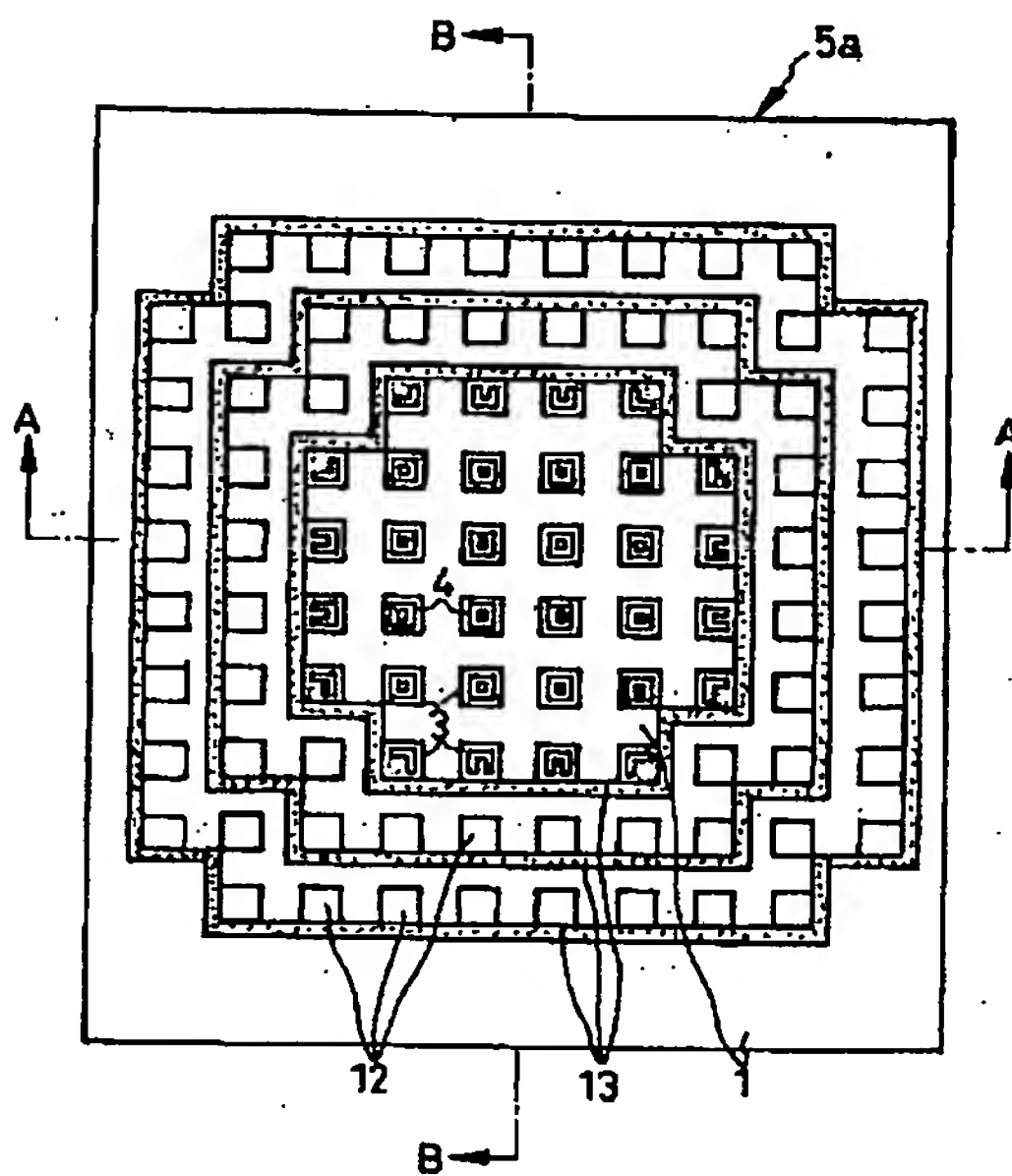
【図1】



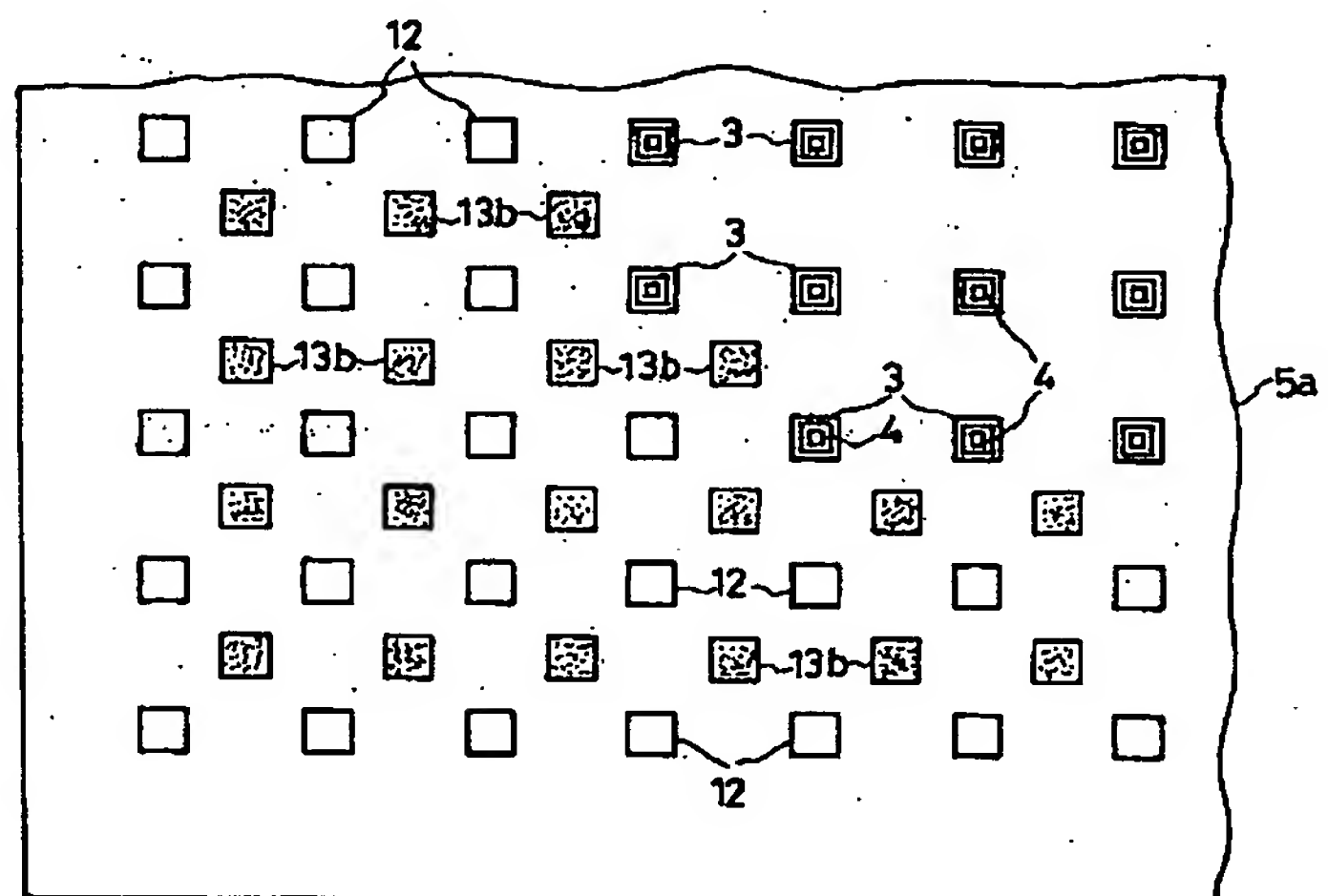
【図6】



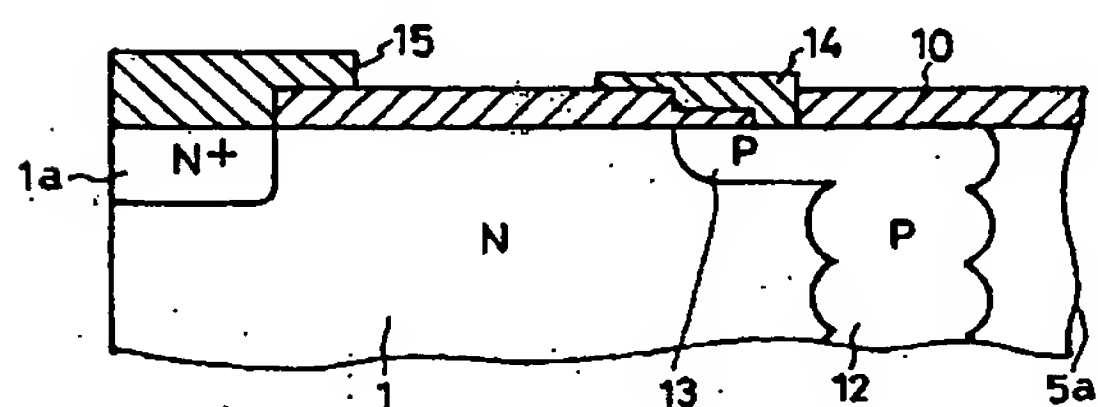
【図2】



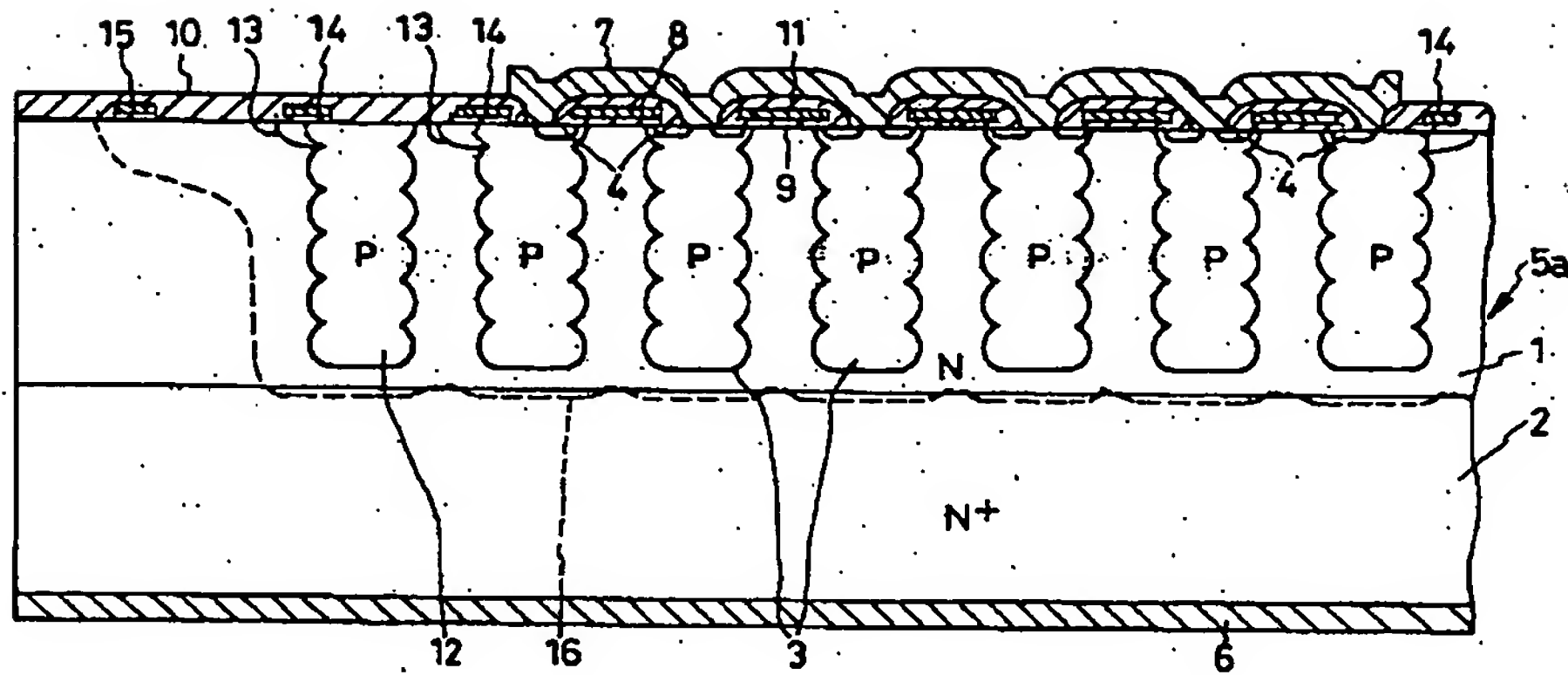
【図5】



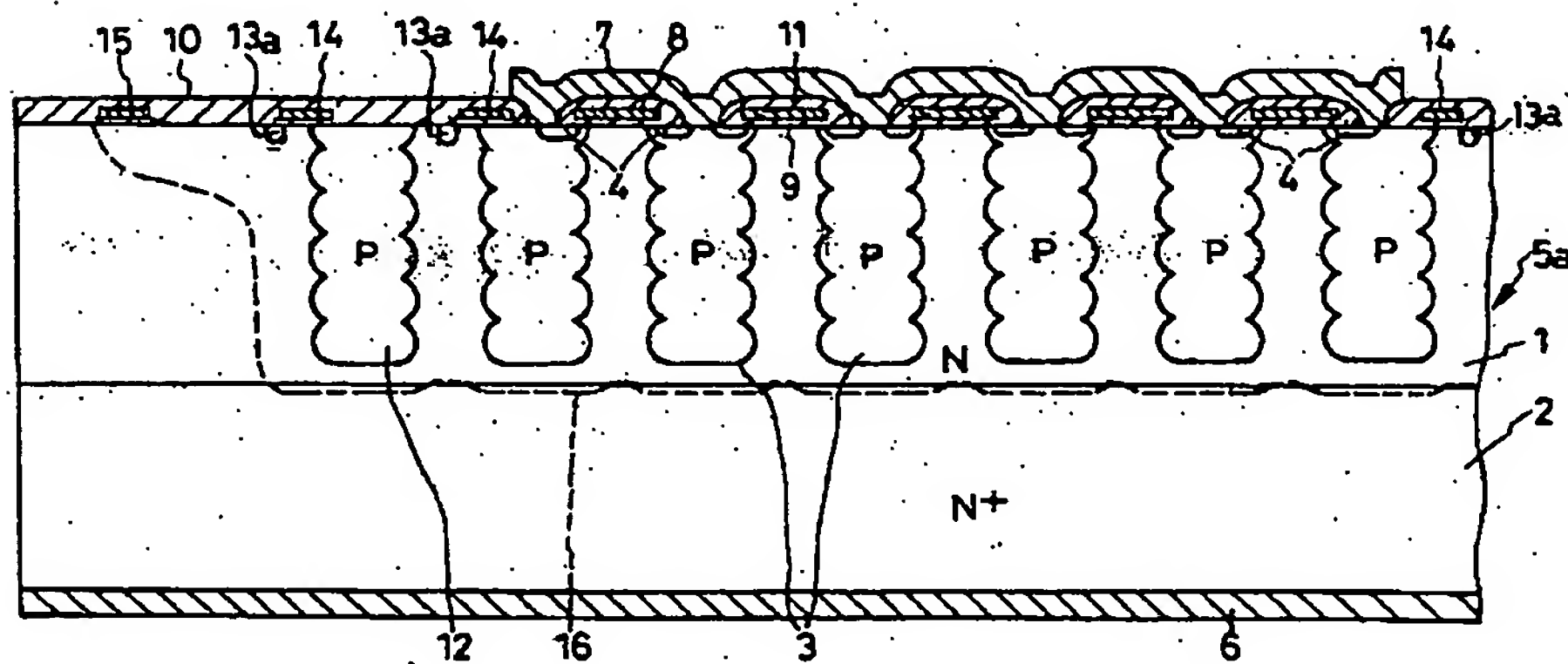
【図7】



【図3】



【図4】



【手続補正書】

【提出日】平成12年3月3日(2000. 3. 3)

【手続補正1】

【補正対象書類名】明細書

【補正対象項目名】特許請求の範囲

【補正方法】変更

【補正内容】

【特許請求の範囲】

【請求項1】 ドレイン領域とドリフト領域と複数のベース領域と複数のソース領域と複数の耐圧向上用領域と補助領域とを有する半導体基体と、ゲート絶縁膜と、ドレイン電極と、ソース電極と、ゲート電極とを備え、前記ドリフト領域は前記ドレイン領域の不純物濃度よりも低い不純物濃度を有し且つ前記半導体基体的一方の主面に露出する部分を有するように配置され、前記ドレイン領域は前記ドリフト領域と前記半導体基体

の他方の主面との間に配置され、

前記複数のベース領域のそれぞれは前記ドリフト領域の中に島状に分散配置され前記複数のエミッタ領域のそれぞれは前記複数のベース領域の中に島状に配置され、前記複数の耐圧向上用領域のそれぞれは前記ベース領域と同一の導電型を有して前記ドリフト領域の中に島状に形成され且つ平面的に見て前記ベース領域の外側に分散配置され且つ前記ベース領域と同じ深さを有し、前記補助領域は前記耐圧向上用領域の近傍の空乏層の広がりを補助するためのものであって、前記耐圧向上用領域と同一の導電型を有し且つ前記半導体基体の表面に露出するように前記ドリフト領域の中に形成され且つ前記耐圧向上用領域よりも浅く形成され且つ平面的に見て前記複数のベース領域の外周側に配置され、前記ドレイン電極と前記ソース電極との間に電圧が印加された時に、前記複

数のベース領域、前記複数の耐圧向上用領域、及び前記補助領域に隣接している前記ドリフト領域のそれぞれの部分に生じる空乏層が互いに連続するように前記複数のベース領域と前記複数の耐圧向上用領域と前記補助領域とが配置されていることを特徴とする絶縁ゲート型電界効果トランジスタ。

【請求項 2】 更に、平面的に見て前記複数のベース領域を囲むようにフィールドプレートと等電位リングとのいずれか一方又は両方を有することを特徴とする請求項 1 記載の絶縁ゲート型電界効果トランジスタ。

【手続補正 2】

【補正対象書類名】明細書

【補正対象項目名】0005

【補正方法】変更

【補正内容】

【0005】

【課題を解決するための手段】上記課題を解決し、上記目的を達成するための発明は、ドレイン領域とドリフト領域と複数のベース領域と複数のソース領域と複数の耐圧向上用領域と補助領域とを有する半導体基体と、ゲート絶縁膜と、ドレイン電極と、ソース電極と、ゲート電極とを備え、前記ドリフト領域は前記ドレイン領域の不純物濃度よりも低い不純物濃度を有し且つ前記半導体基体の一方の主面に露出する部分を有するように配置され、前記ドレイン領域は前記ドリフト領域と前記半導体基体の他方の主面との間に配置され、前記複数のベース領域のそれぞれは前記ドリフト領域の中に島状に分散配置され、前記複数のエミッタ領域のそれぞれは前記複数のベース領域の中に島状に配置され、前記複数の耐圧向上用領域のそれぞれは前記ベース領域と同一の導電型を有して前記ドリフト領域の中に島状に形成され且つ平面的に見て前記ベース領域の外側に分散配置され且つ前記ベース領域と同じ深さを有し、前記補助領域は前記耐圧向上用領域の近傍の空乏層の広がりを補助するためのものであって、前記耐圧向上用領域と同一の導電型を有し

且つ前記半導体基体の表面に露出するように前記ドリフト領域の中に形成され且つ前記耐圧向上用領域よりも浅く形成され且つ平面的に見て前記複数のベース領域の外周側に配置され、前記ドレイン電極と前記ソース電極との間に電圧が印加された時に、前記複数のベース領域、前記複数の耐圧向上用領域、及び前記補助領域に隣接している前記ドリフト領域のそれぞれの部分に生じる空乏層が互いに連続するように前記複数のベース領域と前記複数の耐圧向上用領域と前記補助領域とが配置されていることを特徴とする絶縁ゲート型電界効果トランジスタに係わるものである。

【手続補正 3】

【補正対象書類名】明細書

【補正対象項目名】0006

【補正方法】変更

【補正内容】

【0006】なお、請求項 2 に示すように、フィールドプレート又は等電位リング（EQR）を形成することが望ましい。

【手続補正 4】

【補正対象書類名】明細書

【補正対象項目名】0007

【補正方法】変更

【補正内容】

【0007】

【発明の効果】各請求項の発明によれば FET 素子の周辺耐圧を容易且つ良好に向上させることができる。即ち、ベース領域の外周側にベース領域と同一の深さの耐圧向上用領域を設け、更に耐圧向上用領域よりも浅い補助領域を設けたので、FET 素子の外周側に空乏層を良好に広げることができ、素子周辺耐圧が良好に向上する。また、請求項 2 に示すようにフィールドプレートと等電位リング（EQR）とのいずれか一方又は両方を設けると、空乏層の広がりが更に良好になる。